National Semiconductor

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ADC0831/ADC0832/ADC0834/ADC0838
8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or µPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

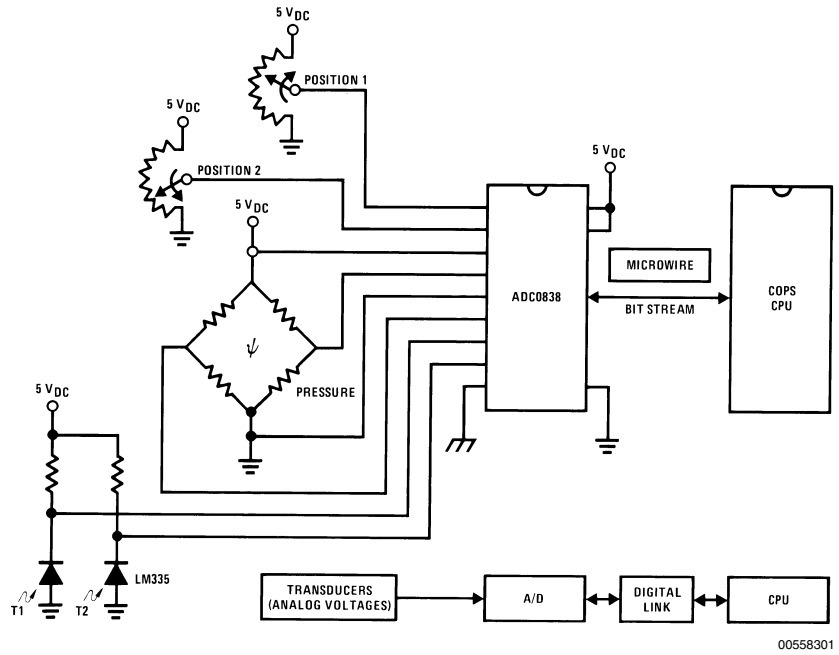
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)
- Surface-Mount Package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 µs

Typical Application



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Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831CCN	1	±1	Molded (N)	0˚C to +70˚C
ADC0831CCWM			SO(M)	0˚C to +70˚C
ADC0832CIWM	2	±1	SO(M)	–40˚C to +85˚C
ADC0832CCN			Molded (N)	0˚C to +70˚C
ADC0832CCWM			SO(M)	0˚C to +70˚C
ADC0834BCN	4	±½	Molded (N)	0˚C to +70˚C
ADC0834CCN		±1	Molded (N)	0˚C to +70˚C
ADC0834CCWM			SO(M)	0˚C to +70˚C
ADC0838BCV	8	±½	PCC (V)	0˚C to +70˚C
ADC0838CCV		±1	PCC (V)	0˚C to +70˚C
ADC0838CCN			Molded (N)	0˚C to +70˚C
ADC0838CIWM			SO(M)	–40˚C to +85˚C
ADC0838CCWM			SO(M)	0˚C to +70˚C

See NS Package Number M14B, M20B, N08E, N14A, N20A or V20A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Current into V^+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package	±20 mA
Storage Temperature	−65˚C to +150˚C
Package Dissipation at T_A=25˚C (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	260˚C
Molded Chip Carrier Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
ESD Susceptibility (Note 5)	2000V

Operating Ratings (Notes 1, 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0832/8CIWM	−40˚C to +85˚C
ADC0834BCN, ADC0838BCV, ADC0831/2/4/8CCN, ADC0838CCV, ADC0831/2/4/8CCWM	0˚C to +70˚C

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \le V_{CC}$ +0.1V, $T_A = T_j$ = 25˚C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	CIWM Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF}=5.00 V							
ADC0838BCV	(Note 6)					±½	**±½**	
ADC0834BCN						±½	**±½**	LSB
ADC0838CCV						±1	**±1**	(Max)
ADC0831/2/4/8CCN						±1	**±1**	
ADC0831/2/4/8CCWM						±1	**±1**	
ADC0832/8CIWM			**±1**					
Minimum Reference Input Resistance (Note 7)		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance (Note 7)		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range (Note 8)			**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Range (Note 8)			**GND −0.05**			GND −0.05	**GND−0.05**	V
DC Common-Mode Error		±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Change in zero error from V_{CC}=5V to internal zener operation (Note 3)	15 mA into V+ V_{CC}=N.C. V_{REF}=5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V_+) (Note 3) MIN	15 mA into V+		**6.3**			6.3	**6.3**	
MAX			**8.5**			8.5	**8.5**	V

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \leq V_{CC}$ +0.1V, $T_A = T_j = 25^{\circ}C$, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.** (Continued)

Parameter	Conditions	CIWM Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Power Supply Sensitivity	V_{CC}=5V±5%	±1/16	**±¼**	±¼	±1/16	±¼	**±¼**	LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel=5V, Off Channel=0V		–0.2 **–1**			–0.2	**–1**	µA
	On Channel=0V, Off Channel=5V		+0.2 **+1**			+0.2	**+1**	µA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel=0V, Off Channel=5V		–0.2 **–1**			–0.2	**–1**	µA
	On Channel=5V, Off Channel=0V		+0.2 **+1**			+0.2	**+1**	µA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC}=5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC}=4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN}=5.0V	0.005	**1**		0.005	1	**1**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN}=0V	–0.005	**–1**		–0.005	–1	**–1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC}=4.75V I_{OUT}=–360 µA I_{OUT}=–10 µA		 **2.4** **4.5**			 2.4 4.5	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC}=4.75V I_{OUT}=1.6 mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT}=0V V_{OUT}=5V	–0.1 0.1	**–3** **3**		–0.1 0.1	–3 +3	**–3** **+3**	µA µA
I_{SOURCE}, Output Source Current (Min)	V_{OUT}=0V	–14	**–6.5**		–14	–7.5	**–6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT}=V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

AC Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f$ = 20 ns and 25˚C unless otherwise specified.

Parameter		Conditions	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle	Min				40	%
(Note 10)	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0} — CLK Falling		C_L=100 pF				
Edge to Output Data Valid		Data MSB First	650		1500	ns
(Note 11)		Data LSB First	250		600	ns
t_{1H}, t_{0H}, — Rising Edge of		C_L=10 pF, R_L=10k	125		250	ns
CS to Data Output and		(see TRI-STATE® Test Circuits)				
SARS Hi–Z		C_L=100 pf, R_L=2k		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground plugs.

Note 3: Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See *Figure 3* in Functional Description Section 6.0)

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 7: Cannot be tested for ADC0832.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 µs. The maximum time the clock can be high is 60 µs. The clock can be stopped when low so long as the analog input voltage remains stable.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Note 12: Typicals are at 25˚C and represent most likely parametric norm.

Note 13: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 14: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Functional Description

1.0 multiplexer Addressing

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "–" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "–" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838 can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "–" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE 1. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC0831	1	1	8
ADC0832	2	1	8
ADC0834	4	2	14
ADC0838	8	4	20

Functional Description (Continued)

TABLE 2. MUX Addressing: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

TABLE 3. MUX Addressing: ADC0838

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0		1		2		3	
		1	0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE 4. MUX Addressing: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

TABLE 5. MUX Addressing: ADC0834

Differential MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

Functional Description (Continued)

TABLE 6. MUX Addressing: ADC0832
Single-Ended MUX Mode

MUX Address		Channel #	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

TABLE 7. MUX Addressing: ADC0832
Differential MUX Mode

MUX Address		Channel #	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
0	0	+	−
0	1	−	+

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{\text{CS}}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.