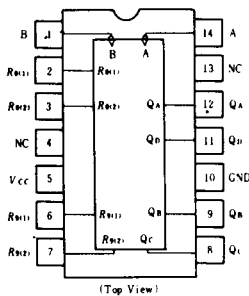


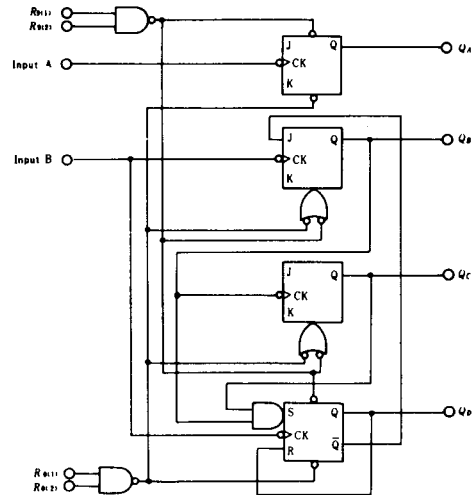
# HD74LS90 • Decade Counters

The HD74LS90 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-stage binary counter for divide-by-five. This device has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications. To use this maximum count length of this counter the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from HD-74LS90 counter by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

## ■ PIN ARRANGEMENT



## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	7.0	V
Input voltage	R Inputs	7.0	V
	A, B Inputs	5.5	V
Operating temperature range	$T_{opr}$	-20 ~ +75	°C
Storage temperature range	$T_{stg}$	-65 ~ +150	°C

## ■ FUNCTION TABLE

Reset/Count Function Table

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{0(3)}$	$R_{0(4)}$	$Q_D$	$Q_C$	$Q_B$	$Q_A$
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

BCD Count Sequence(Notes1)

Count	Outputs			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary Count Sequence(Notes2)

Count	Outputs			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

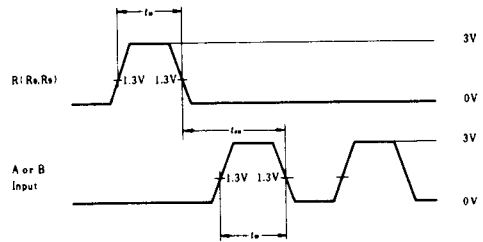
- Notes) 1. Output  $Q_A$  is connected to input B for BCD count.  
 2. Output  $Q_D$  is connected to input A for Bi-Quinary count.  
 3. H; high level, L; low level, X; irrelevant.

# HD74LS90

## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Count frequency	A input	0	—	32	MHz
	B input	0	—	16	
Pulse width	A input	15	—	—	ns
	B input	30	—	—	
	Reset inputs	15	—	—	
Setup time	$t_{su}$	25	—	—	ns

## TIMING DEFINITION



## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit		
Input voltage	$V_{IH}$		2.0	—	—	V		
	$V_{IL}$		—	—	0.8	V		
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	—	—	V		
	$V_{OL}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$						
Input current	Any Reset	$I_{IL}$	$V_{CC} = 5.25\text{V}$ , $V_I = 0.4\text{V}$	—	—	-0.4	mA	
	A input			—	—	-2.4		
	B input			—	—	-3.2		
	Any Reset	$I_{IH}$	$V_{CC} = 5.25\text{V}$ , $V_I = 2.7\text{V}$	—	—	20	$\mu\text{A}$	
	A input			—	—	40		
	B input			—	—	80		
	Any Reset	$I_I$	$V_{CC} = 5.25\text{V}$	$V_I = 7\text{V}$	—	—	0.1	mA
	A input			$V_I = 5.5\text{V}$	—	—	0.2	
B input				—	—	0.4		
Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA		
Supply current * * *	$I_{CC}$	$V_{CC} = 5.25\text{V}$	—	9	15	mA		
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}$ , $I_{IN} = -18\text{mA}$	—	—	-1.5	V		

\*  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

\*\*  $Q_A$  output is tested at specified  $I_{OL}$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan out capability.

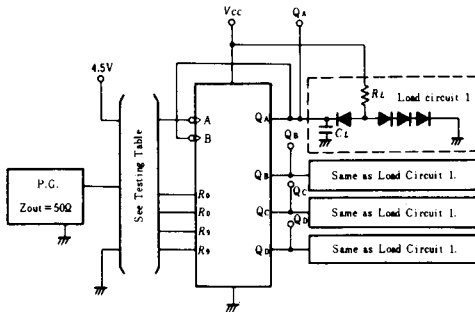
\*\*\*  $I_{CC}$  is measured with all outputs open, both  $R_o$  inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}$ , $T_a = 25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	$f_{max}$	A	$Q_A$	$C_L = 15\text{pF}$ , $R_L = 2\text{k}\Omega$	32	42	—	MHz
		B	$Q_B$		16	—	—	
Propagation delay time	$t_{PLH}$	A	$Q_A$		—	10	16	ns
			$Q_B$		—	12	18	
	$t_{PHL}$	B	$Q_D$		—	32	48	ns
			$Q_B$		—	34	50	
	$t_{PLH}$	B	$Q_B$		—	10	16	ns
			$Q_C$		—	14	21	
	$t_{PHL}$	B	$Q_C$		—	21	32	ns
			$Q_D$		—	23	35	
	$t_{PLH}$	B	$Q_D$	—	21	32	ns	
			$Q_A$	—	23	35		
	$t_{PHL}$	Set-to-0	$Q_A \sim Q_D$	—	26	40	ns	
			$Q_B, Q_C$	—	20	30		
$t_{PHL}$	Set-to-9	$Q_A, Q_D$	—	26	40	ns		
		$Q_B, Q_C$	—	26	40			

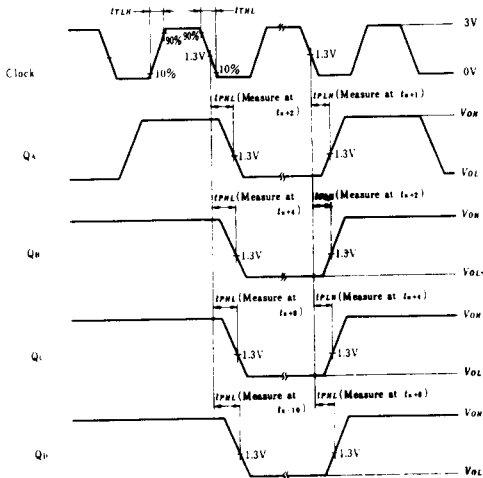
## TESTING METHOD

### 1) Test Circuit



- Notes) 1. Input pulse:  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle=50%  
 2.  $C_L$  includes probe and jig capacitance.  
 3. All diodes are 1S2074  $\text{\textcircled{G}}$ .

**Waveform-1**  $f_{max}$ ,  $I_{PLH}$ ,  $I_{PHL}$ (Clock  $\rightarrow$  Q)



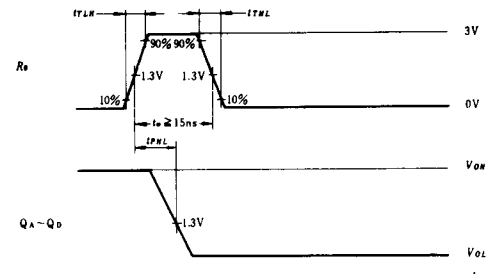
- Notes) 1. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 5\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle=50% and: for  $f_{max}$ ,  $t_{TLH} = t_{THL} \leq 2.5\text{ns}$ .  
 2.  $t_H$  is reference bit time when all outputs are low.

### 2) Testing Table

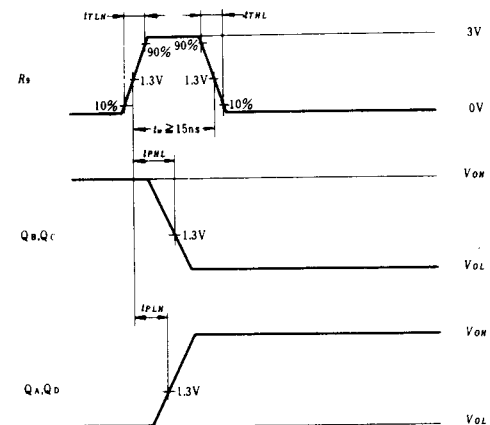
Item	From input to output	Inputs				Outputs			
		A	B	R <sub>0</sub>	R <sub>9</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
$f_{max}$	A $\rightarrow$ Q	IN	to Q <sub>A</sub>	GND	GND	Out	Out	Out	Out
	B $\rightarrow$ Q	4.5V	IN	GND	GND	Out	Out	Out	Out
$I_{PLH}$	A $\rightarrow$ Q <sub>A</sub>	IN	to Q <sub>A</sub>	GND	GND	Out	—	—	—
	A $\rightarrow$ Q <sub>D</sub>	IN	to Q <sub>A</sub>	GND	GND	—	—	—	Out
$I_{PHL}$	B $\rightarrow$ Q <sub>B</sub>	4.5V	IN	GND	GND	—	Out	—	—
	B $\rightarrow$ Q <sub>C</sub>	4.5V	IN	GND	GND	—	—	Out	—
	B $\rightarrow$ Q <sub>D</sub>	4.5V	IN	GND	GND	—	—	—	Out
	R <sub>0</sub> $\rightarrow$ Q	IN*	to Q <sub>A</sub>	IN	GND	Out	Out	Out	Out
	R <sub>9</sub> $\rightarrow$ Q	IN*	to Q <sub>A</sub>	GND	IN	Out	Out	Out	Out

- \*. For initialized  
 \*\*. Measured with each input and unused inputs at 4.5V.

**Waveform-2**  $I_{PHL}$ (R<sub>0</sub>  $\rightarrow$  Q)



**Waveform-3**  $I_{PLH}$ ,  $I_{PHL}$ (R<sub>9</sub>  $\rightarrow$  Q)



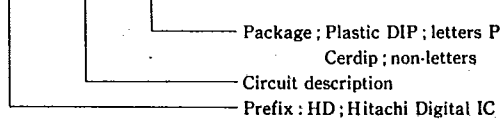
- Notes) 1.  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 5\text{ns}$ .

# PACKAGING INFORMATIONS

T-90-20

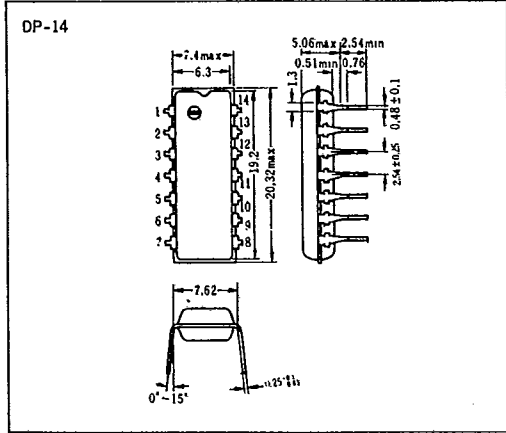
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

## HD 74LS00 P

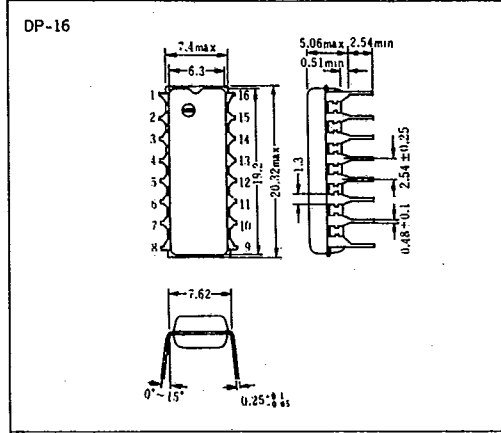


### ■ Plastic DIP

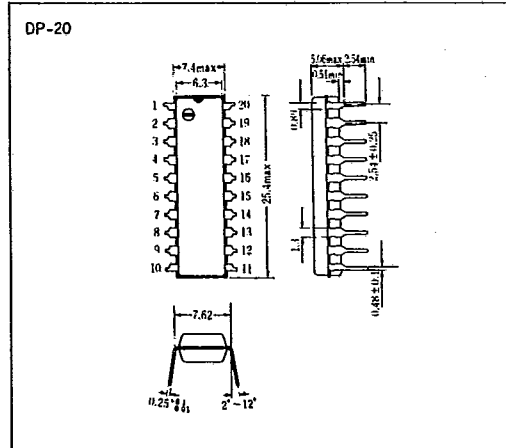
#### ● 14 Pin



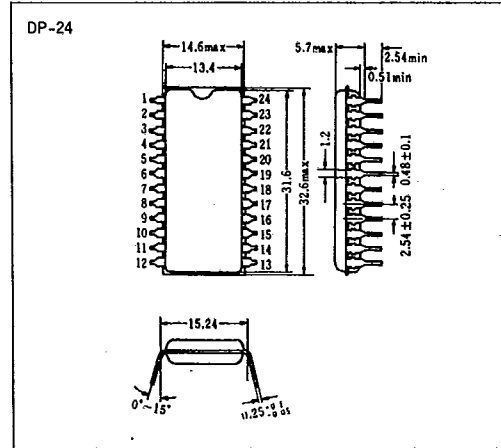
#### ● 16 Pin



#### ● 20 Pin



#### ● 24 Pin

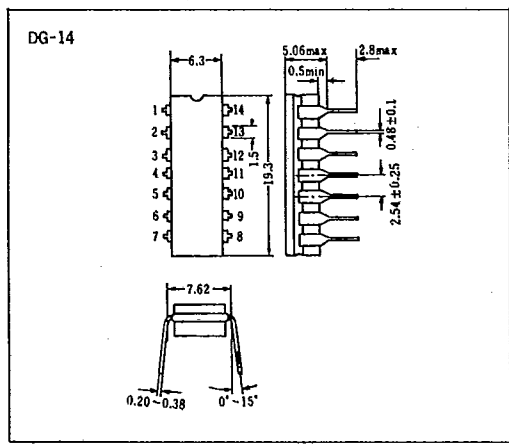


T-90-20

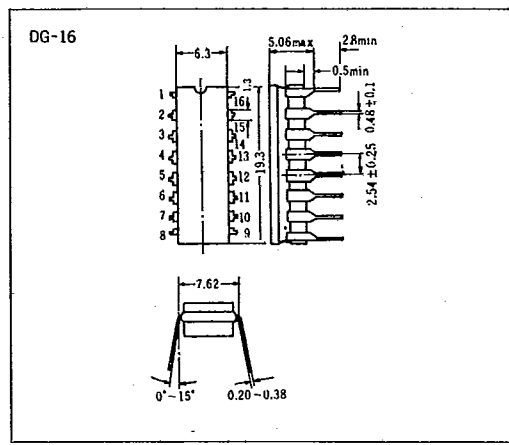
PACKAGING INFORMATIONS

■ Cerdip

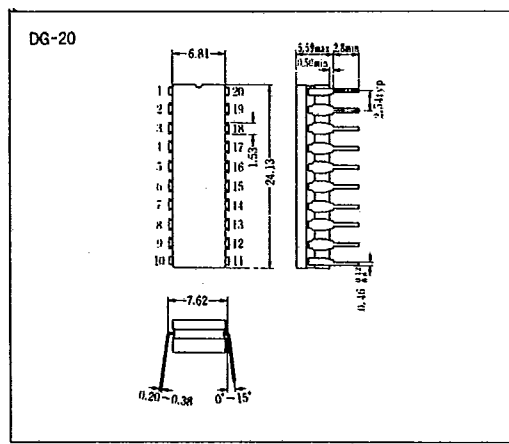
● 14 Pin



● 16 Pin



● 20 Pin



● 24 Pin

